What is claimed :

1. A method of operating a memory system comprising:
programming even columns of addresses of a memory array to a first logic state;
programming odd columns of addresses of a memory array to an opposite logic state;
monitoring logic states in global bit lines; and
simultaneously determining short circuits in local and global bit lines in response to a pattern of logic states in the global bit lines.

2. The method of claim 1 wherein any output of the memory array not comprising a series of alternating states indicates a short in either a local or global bit line.

3. The method of claim 1 wherein monitoring the output of the memory array comprises monitoring the state of global bit lines.

4. The method of claim 1 and further including indicating a short when a global bit line logic state is an inverse state of what was programmed.

5. The method of claim 1 wherein the predetermined test pattern comprises alternating logic high and low states.

6. The method of claim 1 wherein the memory array is a floating gate memory array and the alternating logical high and low states are comprised of a charge and a lack of charge on the floating gate.

7. The method of claim 1 and further including:
selectively coupling odd local bit lines to odd global bit lines; and
selectively coupling even local bit lines to even global bit lines.

8. The method of claim 7 wherein select transistors are coupled between the local bit lines and the global bit lines.

9. The method of claim 7 wherein selectively coupling odd local bit lines comprises coupling a first group of alternating local bit lines to a first global bit line and selectively coupling even local bit lines comprises coupling a second group of alternating local bit lines to a second global bit line.

10. The method of claim 7 wherein selectively coupling odd local bit lines comprises activating a first select transistor that is coupled between a first even local bit line and a first even global bit line.

11. The method of claim 7 wherein selectively coupling comprises:
generating an activation signal coupled to a control gate of a select transistor; and
the select transistor coupling a first even local bit line to a first even global bit line in response to the activation signal.

12. The method of claim 7 wherein selectively coupling comprises:
generating a plurality of activation signals, each signal coupled to a different select transistor of a plurality of select transistors; and
the plurality of select transistors selectively coupling the even local bit lines to the even global bit lines and the odd local bit lines to the odd global bit lines in response to the activation signals.

13. The method of claim 7 wherein the integrated circuit memory is a flash memory device.

14. A method of operating a flash memory comprising:

programming even columns of addresses of a group of memory cells of a memory array to a first logic state;

programming odd columns of addresses of a group of memory cells of a memory array to a second logic state that is inverse to the first logic state;

monitoring the output of the group of memory cells of the memory array; and

detecting local bit line shorts and all global bit lines shorts in response to a pattern of logic states in the global bit lines.

15. The method of claim 14 and further including indicating a short when a global bit line logic state is an inverse logic state of what was programmed into an associated memory cell of the plurality of memory cells.